REMARKS

The Office Action mailed September 13, 2007 has been carefully considered. Reconsideration in view of the following remarks is respectfully requested.

Claim Status and Amendment of the Claims

Claims 1-18 are currently pending.

No claims stand allowed.

The Applicants are grateful for the indication of allowability of claims 2-18, subject to their re-writing in independent form.

Claim 3 has been amended to further particularly point out and distinctly claim subject matter regarded as the invention. Support for these changes may be found in the specification, figures, and claims as originally filed. The text of claims 4-14 and 16-18 is unchanged, but their meaning is changed because they depend from amended claims.

Informal Objections

Claim 3 stands objected to for various informalities.[1] With this Amendment, Claim 3 has been amended to correct the informalities. Withdrawal of the objection to Claim 3 is respectfully requested.

With this Amendment it is respectfully submitted the claims satisfy the statutory requirements.

[1] Office Action mailed September 13, 2007.

The First 35 U.S.C. § 102 Rejection

Claim 1 stands rejected under 35 U.S.C. § 102(b) as allegedly being anticipated by Cloutier.[2] [3] This rejection is respectfully traversed.

According to the M.P.E.P., a claim is anticipated under 35 U.S.C. § 102(a), (b) and (e) only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference.[4]

Claim 1

Claim 1 recites:

> Component with a dynamically reconfigurable architecture for processing data comprising a data processing block TD and a general controller CG capable of controlling the data processing block TD characterized in that:
> - the block TD comprises a plurality of reconfigurable elementary data processing blocks BE; each elementary block BE comprises two inputs, E1 and E2 for reception of data to be processed, and one output S for transmission of processed data; a common input data bus being capable of transmitting data to be processed to the input E1 of each of the blocks BE and the controller CG; for each block BE, an output data bus connected to its output S, being capable of transmitting processed data outside the component and through a bypass data bus to the input E2 of a single other block BE;
> - the controller CG is capable of initializing configurations of blocks BE and controlling their dynamic reconfiguration, controlling data flows at the output from each block BE so as to transmit data either towards the outside or to the input E2 of another block BE, and controlling data flows at the input of each block BE.

The Examiner states:

> ... Cloutier teaches all claimed features in Figs. 1 and 2, component with a dynamically reconfigurable architecture for processing data (Fig. 1) comprising a data processing block TD (102) and a general controller CG (106, 108, 110, 112,

[2] U.S. Patent No. 5,892,962 to Cloutier.
[3] Office Action at ¶ 3.
[4] Manual of Patent Examining Procedure (MPEP) § 2131. See also *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).

> 114 and a host computer) capable of controlling the data processing block TD characterized in that: the block TD comprises a plurality of reconfigurable elementary data processing blocks BE (104s); each elementary block BE comprises two inputs, E1 and E2 (Fig. 2, EAST CONNECTION and WEST CONNECTION) for reception of data to be processed, and one output S (Fig. 2, NORTH CONNECTION) for transmission of processed data; a common input data bus (global bus 114; col. 2, lines 56-59) being capable of transmitting data to be processed to the input E1 of each of the blocks BE (104) and the controller CG (106, 108, 110, 112, 114 and a host computer); for each block BE, an output data bus connected to its output S (SOUTH CONNECTION), being capable of transmitting processed data outside the component and through a bypass data bus to the input E2 of a single other block BE (from an upper left corner 104 to a bottom left comer 104); the controller CG is capable of initializing configurations (col. 6; lines 3540) of blocks BE and controlling their dynamic reconfiguration, controlling data flows(performed by 106, 108, 110, 112, 114 and a host computer) at the output from each block BE so as to transmit data either towards the outside or to the input E2 of another block BE, and controlling data flows at the input of each block BE.[5]

The Applicants respectfully disagree for the reasons set forth below.

Contrary to the Examiner's statement, Cloutier does not disclose a data processing block TD as claimed in Claim 1. In support of the Examiner's contention, the Examiner attempts to equate the data processing block TD of Claim 1, with the FPGA block in Cloutier. The Applicant respectfully submit the Examiner's attempt to equate the data processing block TD of Claim 1, with the FPGA block in Cloutier is improper, as there is no such correspondence. There are several structural and functional differences between the data processing block TD of Claim 1, and the FPGA block of Cloutier.

In Cloutier, the FPGA block does not correspond to a data processing block TD. The FPGA block of Cloutier consists of a set of 4 PE (Programmable elements), whereas the data processing block TD of Claim 1 requires a combination of elementary blocks BE, each of which comprises two inputs for reception of data to be processed, and one output for transmission of

[5] Office Action dated September 13, 2007, ¶ 3.

processed data. Claim 1 further requires for each block BE, an output data bus connected to its output S, being capable of transmitting processed data outside the component and through a bypass data bus to the input E2 of a single other block BE. This structural difference results in a difference in operation between the FPGA block of Cloutier and the data processing block TD of Claim 1.

In the embodiment claimed in Claim 1, two control levels are possible. The first control level is a local control carried out by elementary processing units within each elementary block BE. The second control level is a global control carried out by the general controller CG. Whereas Cloutier's architecture allows only one global control level.

Moreover, the connections between the elementary processing units PE (see figures 4, 5, and 7 of the specification) are completely different from those of Cloutier's structure (see figure 3 of Cloutier). As a result, in the claimed component of the applicant's invention, the controller CG is capable of initializing the configurations of blocks BE block-by-block, and dynamically controlling the reconfiguration of the blocks BE block-by-block so as to allow the block TD to process data in a pipeline mode, in a parallel mode, or in a combined mode.

Another advantage of the Applicant's invention as presently claimed is that for controlling the operations of the blocks BE, the controller CG needs to send only simplified instructions (context numbers) to the blocks BE; complex instructions are managed locally by the elementary processing units. This feature allows flexibility and dynamic routing at the elementary processing units level and at each processing cycle, while Cloutier's architecture is limited to a fixed routing. Whereas in Cloutier's architecture, the FPGA receives complex instructions directly from the CG.

For the above reasons, the 35 U.S.C. § 102 rejection of Claim 1 based on Cloutier is unsupported by the cited art of record. Thus, a *prima facie* case has not been established and the rejection must be withdrawn.

Claims 2-18

Claims 2-18 depend from Claim 1. Claim 1 being allowable, Claims 2-18 must also be allowable for at least the same reasons as Claim 1.

In view of the foregoing, it is respectfully asserted that the claims are now in condition for allowance.

Conclusion

It is believed that this Amendment places the above-identified patent application into condition for allowance. Early favorable consideration of this Amendment is earnestly solicited.

If, in the opinion of the Examiner, an interview would expedite the prosecution of this application, the Examiner is invited to call the undersigned attorney at the number indicated below.

The Applicants respectfully request that a timely Notice of Allowance be issued in this case.

Please charge any additional required fee or credit any overpayment not otherwise paid or credited to our deposit account No. 50-1698.

Respectfully submitted,

THELEN REID BROWN
RAYSMAN & STEINER LLP

Dated: December 13, 2007

John P. Schaub
Reg. No. 42,125

THELEN REID BROWN RAYSMAN & STEINER LLP
P.O. Box 640640
San Jose, CA 95164-0640
Tel. (408) 292-5800
Fax. (408) 287-8040